REMARKS / ARGUMENTS

Claims 1-30 are pending in the application.

Claims 1-4, 7-12, 14, 16-20, 25-27, and 29-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S Patent No. 5,860,105 to McDermott (Hereinafter "McDermott") in view of U.S Patent No. 6,490,657 to Masubuchi et al. (Hereinafter "Masubuchi"). Claims 5-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over McDermott in view of Masubuchi in further view of U.S Patent No. 6,058,456 to Arimilli (Hereinafter "Arimilli"). Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over McDermott in view of Masubuchi in further view of U.S Patent No. 6,460,122 to Otterness et al. (Hereinafter "Arimilli"). Claims 15 and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over McDermott in view of Masubuchi in further view of U.S Patent No. 5,724,550 to Stevens (Hereinafter "Stevens"). Claims 5-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Masubuchi in view of McDermott.

Claim Rejections under 35 U.S.C. §103(a)

Claims 1-4, 7-12, 14, 16-20, 25-27, and 29-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over McDermott in view of Masubuchi. McDermott discloses an NDIRTY cache line lookahead technique used to expedite cache flush and export operations by providing a mechanism to avoid scanning at least some cache lines that do not contain dirty data (*See* Abstract). Masabuchi discloses addresses of all of dirty blocks of a cache memory are, by an update address registering section, stored in one of plural regions of an update address memory (*See* Abstract).

Neither McDermott nor Masabuchi disclose a list structure for tracking a status of a plurality of cache entries, wherein the list structure is located outside a cache and does not contain cache data or addresses. McDermott discloses a list structure located internal to the cache. Specifically, McDermott states:

> Referring to FIG. 2a, the NDIRTY cache line lookahead technique of the invention is implemented as part of the flush/export logic for the L1 cache 204.

(McDermott, Col. 6, Lines 57-59).

While this list structure does not have cache data and address, that is because the list is an integral part of the cache. Masabuchi discloses an external address list structure. Specifically, Masabuchi states:

> A cache flush device 30 and a memory controller 50 for a main memory 51, are connected to the system bus 40. The cache flush device 30 includes a system bus interface 31, an update address memory 32 (consisting of regions A.sub.0 to A.sub.n-1), an update address registering section 33, an update address removing section 34 and a flush executing section 35. The update address registering section 33 and the update address removing section 34 can be implemented as a single hardware module.
>
> The system bus interface 31 serves as an interface with the system bus 40.
>
> The update address memory 32 consists of n regions A.sub.0 to A.sub.n-1 for storing addresses of data held in the dirty blocks of the cache memories 20. In this embodiment, if and only if a dirty block holds data of a certain address, the address is stored in a certain region of the update address memory 32. From now on, we call such a memory address stored in the update address memory 32 an update address.

(Masabuchi, Col. 11, Lines 5-23).

The Masabuchi list structure is entirely a list of addresses. The addresses are necessitated by the external nature of the list structure. Combining Masabuchi and McDermott would not produce a workable external list structure that does not contain cache data or addresses. Therefore, a list structure for tracking a status of a plurality of cache entries, wherein the list

structure is located outside a cache and does not contain cache data or addresses, as cited by claims 1, 16, and 21.

Further, neither McDermott or Masabuch provide a motive for combining the references. In fact, McDermott specifically teaches away from such a combination. McDermott states:

> An object of the invention is to store information in a cache array to reduce the time required for cache export and flush (export then invalidate) operations.

(McDermott, Col. 1, Lines 65-67).

McDermott emphasizes storing everything in the cache to improve the speed of the cache. An external list structure would be counter to this teaching.

With respect to other references cited by Examiner, Arimilli, Otterness, and Stevens do not overcome the above noted deficiencies of McDermott and Masubuchi. In particular, Arimilli, Otterness, and Stevens do not teach or suggest "a list structure for tracking a status of a plurality of cache entries, wherein said list structure is located outside a cache and wherein said list structure does not contain cache data or addresses," as recited in independent claims 1 and 21, and currently amended independent claim 16.

Therefore, Applicants assert that independent claims 1, 16, and 21 contain allowable subject matter. Claims 2-15, 17-20, and 22-24 depend from independent claims 1, 16, and 21, respectively, and therefore also contain allowable subject matter. Accordingly, Applicants respectfully request that the rejections to claims 1-24 under 35 U.S.C. §103(a) be withdrawn.

With respect to independent claim 25, for similar reasons stated above, it would not be proper to combine the teaching of McDermott and Masubuchi because the references teach away from each other and should not be combined. Specifically, it would not be obvious to those of skill in the art to create a table of cache entries without addresses or cache data separate from the

cache because no means for associating the table to the cache lines was taught by the prior art or known to those of ordinary skill in the art.

Therefore, Applicants assert that independent claim 25 contains allowable subject matter. Claims 26-30 depend from independent claim 25, and therefore also contains allowable subject matter. Accordingly, Applicants respectfully request that the rejections to claims 25-30 under 35 U.S.C. §103(a) be withdrawn.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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